WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, comprising:

a semiconductor element being formed on a support substrate;

a multi-layer wiring structure being formed in an insulation film on the support substrate, said multi-layer wiring structure comprising at least one connection hole and at least one metal wiring layer; and

a heat conduction part being formed of the same conductive materials as the connection hole and the metal wiring layer, said heat conduction part extending toward an upper layer side along a path different from a wiring path comprising a connection hole and a metal wiring for signal transmission.

2. The semiconductor integrated circuit device as claimed in claim 1, wherein the support

substrate comprises one of a semiconductor substrate and a SOI substrate.

3. The semiconductor integrated circuit device as claimed in claim 1, wherein the heat conduction part comprises an uppermost wiring layer.

4. The semiconductor integrated circuit device as claimed in claim 3, further comprising an aperture on the uppermost wiring layer in the insulation film.

5. The semiconductor integrated circuit device as claimed in claim 1, wherein the semiconductor element comprises a MOS transistor and said MOS transistor comprises one of a fully-depletion type SOI

transistor, a partially-depletion type SOI transistor and a SON transistor.

6. The semiconductor integrated circuit device as claimed in claim 5, wherein the heat conduction part is connected to a gate electrode of the MOS transistor directly or via the connection hole and the metal wiring layer for signal transmission.

7. The semiconductor integrated circuit device as claimed in claim 5, wherein the heat conduction part is connected to one of a source region and a drain region of the MOS transistor directly or via the connection hole and the metal wiring layer for signal transmission.

8. The semiconductor integrated circuit device as claimed in claim 5, wherein the heat conduction part is connected to an element separation film to electrically separate the MOS transistor directly or via the connection hole and the metal wiring layer for signal transmission.

9. The semiconductor integrated circuit device as claimed in claim 1, wherein the heat conduction part comprises at least one dummy metal that is not used as an electric wire, said dummy metal being disposed at the same coordinate for each layer of the multi-layer wiring structure and being connected to each other via a connection hole.

10. A semiconductor integrated circuit device, comprising:

a plurality of semiconductor elements being formed on a support substrate;

a plurality of function modules being formed by modularizing the plurality of semiconductor elements for each function thereof; and

at least one heat conduction part comprising the same conductive materials as a connection hole and a metal wiring layer constituting a multi-layer wiring structure, said heat conduction part extending toward an upper layer side along a path different from a wiring path comprising a connection hole and a metal wiring layer for signal transmission,

wherein at least one of the plurality of function modules comprises one or more of the at least one heat conduction part.

11. The semiconductor integrated circuit device as claimed in claim 10, wherein the heat conduction part is arranged corresponding to heat capacity of a gate electrode of each of the plurality of function modules.

12. The semiconductor integrated circuit device as claimed in claim 10, further comprising:

at least one field cell being disposed in an empty space between the function modules, and

wherein one or more of the at least one field cell comprises one or more of the at least one heat conduction part.

13. The semiconductor integrated circuit device as claimed in claim 12, wherein the field cell having the heat conduction part is disposed corresponding to heat capacity of a gate electrode in a function module.

14. A method of fabricating a standard cell type semiconductor integrated circuit device having a plurality of semiconductor elements, the method

comprising the steps of:

modularizing the plurality of semiconductor elements for each function thereof so as to form a plurality of function modules;

maintaining the plurality of function modules as standard cells in a library; and

arranging the standard cells in the standard cell type semiconductor integrated circuit device,

wherein at least one of the standard cells comprises a heat conduction part, said heat conduction part comprising the same conductive materials as a connection hole and a metal wiring layer constituting a multi-layer wiring structure, said heat conduction part extending toward an upper layer side along a path different from a wiring path comprising a connection hole and a metal wiring layer for signal transmission.

15. The method as claimed in claim 14, wherein the standard cell type semiconductor integrated circuit device comprises at least one field cell being arranged in an empty space between the function modules, said field cell comprising a heat conduction part

comprising the same conductive materials as a connection hole and a metal wiring layer constituting a multi-layer wiring structure, said heat conduction part extending toward an upper layer side along a path different from a wiring path comprising a connection hole and a metal wiring layer for signal transmission.